**Processor Design Project**

**Interim Report**

**EE480**

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# Introduction

The purpose of this project is to design, develop, test, and validate a high performing accumulator based processor capable of efficiently implementing an Instruction Set Architecture (ISA) that we specifically designed for it. By definition, the accumulator based architecture has only one register, called the accumulator, in the data path and for all ALU operations. For every ALU instruction, one operand will always be in the ACC register and the other operand comes from RAM. The process of developing the accumulator processor begins with defining the ISA and designing the physical layout of the architecture. After the architecture is designed, each clock cycle operation of the processor is defined as to show the processors operation and functionality as a system. From this, the steps of each instruction are diagramed on a cycle by cycle basis to define their exact operation by the system on the architecture.

# Instruction Set Architecture Development

The instruction set architecture defines the computer architecture and capabilities by detailing the data types, possible instructions, registers, memory addressing modes, interrupt control, and data input/output control. Defining the instruction set architecture enables programming the computer architecture, assembly instructions and associated parameters are translated to machine code.

## Implementation

This accumulator computer architecture includes 16 opcodes with multiple flags, which describe addressing modes and specific opcode operation. Each instruction is implemented as 16-bits wide (one word) for this accumulator processor, which features an 8-bit data bus. 5-bits are reserved for the opcode, 3-bits are reserved for the opcode flag, and 8-bits are allocated for the operand. Table 1 provides an overview of the instruction structure. The size of the operand is limited by the width of the data bus (5-bits).

Table - Instruction Structure

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | 15:11 | 10:8 | 7:0 |
| Field | OPCODE | FLAG | OPERAND |

Each of the 16 opcodes are detailed in the following sections by OPCode, flags, assembly format, machine code format, description of operation, architecture level operation, and memory addressing.

### Add

|  |  |
| --- | --- |
| Instruction | Add |
| OPCode | 00000 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | ADD FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00000 | xxx | RAM ADDR / INTEGER | |
| Description | Adds the specified operand to the current contents of the ACC register. The Output from the ALU will be returned to the ACC register. |
| Operation | ACC ← ACC + OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Sub

|  |  |
| --- | --- |
| Instruction | SUB |
| OPCode | 00001 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | SUB FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00001 | xxx | RAM ADDR / INTEGER | |
| Description | Subtracts the specified operand from the current contents of the ACC register. The Output from the ALU will be returned to the ACC register. |
| Operation | ACC ← ACC - OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical OR

|  |  |
| --- | --- |
| Instruction | OR |
| OPCode | 00011 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | OR FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00011 | xxx | RAM ADDR / INTEGER | |
| Description | Perform a LOGICAL OR operation of contents in Accumulator and OPERAND. The result of the operation will be stored in the accumulator. |
| Operation | ACC ← ACC | OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical AND

|  |  |
| --- | --- |
| Instruction | AND |
| OPCode | 00100 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | AND FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00100 | xxx | RAM ADDR / INTEGER | |
| Description | Perform a LOGICAL AND operation of contents in Accumulator and OPERAND. The result of the operation will be stored in the accumulator. |
| Operation | ACC ← ACC & OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical Complement (COMP)

|  |  |
| --- | --- |
| Instruction | COMP |
| OPCode | 10000 |
| Flags | 00 |
| Format | COMP FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10000 | 000 | 00000000 | |
| Description | Perform LOGICAL complement/Negation on the contents of the accumulator register. The complement will be stored in the accumulator register. |
| Operation | ACC ← NOT ACC |
| Memory Addressing | N/A |

### Multiply and Divide

|  |  |
| --- | --- |
| Instruction | MUL |
| OPCode | 00010 |
| Flags | 00: Direct 01: Indirect |
| Format | MUL FLAG OPERAND [Lower 4 bits] |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00010 | 000 001 | RAM ADDR | |
| Description | Performs multiplication on lower 4-bits of Accumulator and lower 4-bits of the operand. |
| Operation | ACC ← ACC \* OPERAND |
| Memory Addressing | Direct and Indirect |

|  |  |
| --- | --- |
| Instruction | DIV |
| OPCode | 00010 |
| Flags | 10: Direct 11: Indirect |
| Format | DIV FLAG OPERAND [Lower 4 bits] |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00010 | 010 011 | RAM ADDR | |
| Description | Performs division on lower 4-bits of Accumulator and lower 4-bits of the operand. |
| Operation | ACC ← ACC / OPERAND |
| Memory Addressing | Direct and Indirect |

### Arithmetic Left/Right Shift

|  |  |
| --- | --- |
| Instruction | SHFT |
| OPCode | 00101 |
| Flags | 00: Left Shift in 0 01: Left Shift in 1 |
| Format | SHFT FLAG OPPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00101 | 000 001 | INTEGER < 7 | |
| Description | Performs a LEFT SHIFT operation on the contents of the accumulator register. The value of the bit shifted in is dependent upon the provided flag. Any number of bits less than 7. |
| Operation | ACC ← ACC [N-2:0 + (FLAG BIT)\*OPERAND] |
| Memory Addressing | N/A |

|  |  |
| --- | --- |
| Instruction | SHFT |
| OPCode | 00101 |
| Flags | 10: Right Shift in 0 11: Right Shift in 1 |
| Format | SHFT FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00101 | 010 011 | INTEGER < 7 | |
| Description | Performs a RIGHT SHIFT operation on the contents of the accumulator register. The value of the bit shifted in is dependent upon the provided flag. Shift by any number of bits less than 7. |
| Operation | ACC ← ACC [OPERAND\*(FLAG BIT) + N-1:1] |
| Memory Addressing | N/A |

### Conditional Branch

|  |  |
| --- | --- |
| Instruction | BRA |
| OPCode | 00110 |
| Flags | 00: Branch if Equal 01: Branch if Not Equal |
| Format | BRA FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00110 | 000 001 | MEM ADDR | |
| Description | Performs a comparison between the Accumulator and Operand. If true, jump to instruction pointed to by OPERAND.  The comparison is performed on the ACC and A registers. |
| Operation | PC ←OPERAND |
| Memory Addressing | Direct |

### Unconditional Jump

|  |  |
| --- | --- |
| Instruction | JMP |
| OPCode | 00111 |
| Flags | NULL |
| Format | JUMP OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00111 | 000 | MEM ADDR | |
| Description | Executes an unconditional branch. When encountered the instruction pointer is adjusted to the operand target memory address. |
| Operation | IP ←IP + OPERAND |
| Memory Addressing | N/A |

### Jump/Return to/from a Subroutine

|  |  |
| --- | --- |
| Instruction | RTS |
| OPCode | 01000 |
| Flags | NULL |
| Format | RTS |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01000 | 000 | 00000000 | |
| Description | Transfer program control to the address located in the implied return address. Return is made to the top element in the PC stack. Should also pop the ACC value from the ACC stack. |
| Operation | PC ← Implied Address (From Stack) |
| Memory Addressing | NULL |

### Return from Interrupt Service Routine

|  |  |
| --- | --- |
| Instruction | RTI |
| OPCode | 01001 |
| Flags | NULL |
| Format | RTI |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01001 | 000 | 00000000 | |
| Description | Return from an Interrupt Subroutine to the position the PC was at before the interrupt. The PC location to return to will be the top element in the PC stack. |
| Operation | PC ← Return Address (From Stack) |
| Memory Addressing | NULL |

### LOAD Accumulator

|  |  |
| --- | --- |
| Instruction | LOAD |
| OPCode | 01010 |
| Flags | 00: Direct 01: Indirect  10: Immediate |
| Format | LOAD FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01010 | 000 001 010 | MEM ADDR MEM ADDR Integer | |
| Description | **Direct Mode** Copy the contents of the address in RAM specified by the source operand to the accumulator.  **Indirect Mode:** Copy the accumulator to the destination memory address found at the memory address of the operand  **Immediate Mode:** Copy the 8-bit immediate source operand to the accumulator. |
| Operation | **Direct Mode** ACC ← memory (OPERAND)  **Indirect Mode:**  ACC ← Memory{ memory( OPERAND) }   **Immediate Mode:** ACC ← IMMED OPERAND |
| Memory Addressing | Direct, Immediate |

### STORE Accumulator to RAM

|  |  |
| --- | --- |
| Instruction | STOR |
| OPCode | 01011 |
| Flags | 00: Direct 01: Indirect |
| Format | STORE FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01011 | 000 001 | MEM ADDR | |
| Description | **Direct Mode** Copy the accumulator to the destination memory address specified by the operand **Indirect Mode:** Copy the accumulator to the destination memory address found at the memory address of the operand |
| Operation | **Direct Mode** memory(OPERAND) ← ACC **Indirect Mode:** Memory{ memory( OPERAND) } ← ACC |
| Memory Addressing | Direct, Indirect |

### LOAD A Register from RAM

|  |  |
| --- | --- |
| Instruction | LDA |
| OPCode | 10001 |
| Flags | 00: Direct 01: Indirect  10: Immediate |
| Format | LOAD FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10001 | 000 001 010 | MEM ADDR MEM ADDR Integer | |
| Description | **Direct Mode** Copy the contents of the address in RAM specified by the source operand to the A register.  **Indirect Mode:** Copy the memory data found at the memory address of the operand into the A register.   **Immediate Mode:** Copy the 8-bit immediate source operand to the A register. |
| Operation | **Direct Mode** A ← memory (OPERAND)  **Indirect Mode:**  A ← Memory{ memory( OPERAND) }   **Immediate Mode:** A ← IMMED OPERAND |
| Memory Addressing | Direct, Immediate |

### STORE A Register to RAM

|  |  |
| --- | --- |
| Instruction | STA |
| OPCode | 10010 |
| Flags | 00: Direct 01: Indirect |
| Format | STORE FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10010 | 000 001 | MEM ADDR | |
| Description | **Direct Mode** Copy the A register contents to the destination memory address specified by the operand **Indirect Mode:** Copy the A register contents to the destination memory address found at the memory address of the operand |
| Operation | **Direct Mode** memory(OPERAND) ← A **Indirect Mode:** Memory{ memory( OPERAND) } ← A |
| Memory Addressing | Direct, Indirect |

### LOAD B Register from RAM

|  |  |
| --- | --- |
| Instruction | LDB |
| OPCode | 10011 |
| Flags | 00: Direct 01: Indirect  10: Immediate |
| Format | LOAD FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10011 | 000 001 010 | MEM ADDR MEM ADDR Integer | |
| Description | **Direct Mode** Copy the contents of the address in RAM specified by the source operand to the B register.  **Indirect Mode:** Copy the memory data found at the memory address of the operand into the B register.   **Immediate Mode:** Copy the 8-bit immediate source operand to the B register. |
| Operation | **Direct Mode** B ← memory (OPERAND)  **Indirect Mode:**  B ← Memory{ memory( OPERAND) }   **Immediate Mode:** B ← IMMED OPERAND |
| Memory Addressing | Direct, Immediate |

### STORE B Register to RAM

|  |  |
| --- | --- |
| Instruction | STB |
| OPCode | 10100 |
| Flags | 00: Direct 01: Indirect |
| Format | STORE FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10100 | 000 001 | MEM ADDR | |
| Description | **Direct Mode** Copy the B register contents to the destination memory address specified by the operand **Indirect Mode:** Copy the B register contents to the destination memory address found at the memory address of the operand |
| Operation | **Direct Mode** memory(OPERAND) ← B **Indirect Mode:** Memory{ memory( OPERAND) } ← B |
| Memory Addressing | Direct, Indirect |

### INPUT Data Word to RAM

|  |  |
| --- | --- |
| Instruction | INPUT |
| OPCode | 01100 |
| Flags | 00: Direct 01: Indirect |
| Format | INPUT FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01100 | 000 001 | MEM ADDR | |
| Description | Input a data word to RAM |
| Operation | **Direct Mode** memory(OPERAND) ← I/O Port  **Indirect Mode:** Memory{ memory( OPERAND) } ← I/O Port |
| Memory Addressing | Direct, Indirect |

### OUTPUT Data Word from RAM

|  |  |
| --- | --- |
| Instruction | OUTPUT |
| OPCode | 01101 |
| Flags | 00: Direct 01: Indirect |
| Format | OUTPUT FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01101 | 000 001 | MEM ADDR | |
| Description | Output data word from RAM |
| Operation | **Direct Mode** memory(OPERAND) → I/O Port  **Indirect Mode:** Memory{ memory( OPERAND) } → I/O Port |
| Memory Addressing | Direct, Indirect |

### LOAD Mask Register of HVPI

IN PROGRESS

|  |  |
| --- | --- |
| Instruction | LOAD Mask Register of HVPI |
| OPCode | 01110 |
| Flags |  |
| Format |  |
| Description |  |
| Operation |  |
| Memory Addressing |  |

### NOP

|  |  |
| --- | --- |
| Instruction | NOP |
| OPCode | 01111 |
| Flags | NULL |
| Format | NOP |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01111 | 000 | 00000000 | |
| Description | Performs no operation. |
| Operation | NULL |
| Memory Addressing | NULL |

# Accumulator Architecture Development

## Architecture Overview



Figure - Top Level Architecture Overview



Figure - ACC Processor Single Cycle Diagram

## Instruction Implementation



### Add



Figure - ADD Flow Diagram

### Sub



Figure - SUB Flow Diagram

### Logical OR



Figure - OR Flow Diagram

### Logical AND



Figure - AND Flow Diagram

### Logical Complement (COMP)



Figure - COMP Flow Diagram

### Multiply and Divide



Figure - MULT Flow Diagram



Figure - DIV Flow Diagram

### Arithmetic Left/Right Shift



Figure - SHFT Flow Diagram

### Conditional Branch



Figure - BRA Flow Diagram

### Unconditional Jump



Figure - JMP Flow Diagram

### Jump/Return to/from a Subroutine



Figure - RTS Flow Diagram

### LOAD Accumulator from RAM



Figure - LOAD Flow Diagram

### STORE Accumulator to RAM



Figure - STORE Flow Diagram

### LOAD A Register from RAM



Figure - LDA Flow Diagram

### STORE A Register to RAM



Figure - STA Flow Diagram

### LOAD B Register from RAM



Figure - LDB Flow Diagram

### STORE B Register to RAM



Figure - STB Flow Diagram

### INPUT Data Word to RAM



Figure - INPUT Flow Diagram

### OUTPUT Data Word from RAM



Figure - OUTPUT Flow Diagram

### LOAD Mask Register of HVPI

IN PROGRESS

### NOP



Figure - NOP Flow Diagram

## Direct Mapped Cache



Figure - Direct Mapped Cache Flow Diagram

# Conclusion

# References